REMARKS

Claims 7-14, 19, and 21-38 are pending in the application and are presented for reconsideration and further examination in view of the foregoing amendments and following remarks. Claims 9, 12-14, and 17 have been withdrawn from consideration.

In the outstanding Office Action claims 7-8, 10-11, and 22 were rejected under 35 U.S.C. § 112, 2nd paragraph as indefinite; claims 7, 10, 15, 18-19, and 21 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,341,546 to Akhavain et al.; claim 11 was rejected under 35 U.S.C. § 103(a) as obvious over the Akhavain et al. '546 patent in view of U.S. Patent No. 5,445,308 to Nelson; claims 8, 16, and 20 were rejected under 35 U.S.C. § 103(a) as obvious over the Akhavain et al. '546 patent in view of U.S. Patent No. 5,821,624 to Pasch; and claim 22 was rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,371,328 to Gutierrez;

By this Response and Amendment claims 15-18 and 20 are canceled, claims 7, 11, and 22 are amended to obviate the indefiniteness rejections; claims 7, 19, 21, and 22 are amended to claim that the therein recited method steps are performed --in sequence--; and newly submitted claims 23-38 are added.

Support for newly submitted claims 23-38 is found throughout the originally filed specification. It is therefore respectfully

submitted that the above amendments introduce no new matter within the meaning of 35 U.S.C. § 132.

Rejections Under 35 U.S.C. § 112, 2nd Paragraph

Claims 7-8, 10-11 and 22 were rejected due to errors of antecedent basis.

RESPONSE

Claims 7, 11, and 22 have been amended to obviate the rejections. As amended the rejections are respectfully traversed.

The claims have been amended to correct errors of antecedent basis as noted by the Examiner. Claims 7, 19, and 21 have been amended by changing the terms "integrated circuit" and "integrated circuit chip" to "semiconductor chip"; claim 11 has been amended by deleting the term "in the encapsulant"; and claim 22 has been amended by changing the term "the substrate" to --a substrate-- on line 5 thereof. The rejections of claims 8 and 10 are asserted to be overcome by virtue of the amendment to claim 7.

As amended the errors of antecedent basis are asserted to be corrected. Accordingly, reconsideration and withdrawal of the rejections is respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 7, 10, 15, 18-19, and 21 were rejected as anticipated

by the Akhavain '546 patent; and claim 22 was rejected as anticipated by the Gutierrez '328 patent.

RESPONSE

Claims 15 and 18 have been canceled thereby rendering their rejections moot. Applicants respectfully traverse the remaining rejections.

The test for anticipation under section 102 is whether each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); MPEP §2131. The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP §2131. The elements must also be arranged as required by the claim. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

Claims 7 and 10

Claim 7 has been amended to clarify that the recited method steps are performed in the particular sequence therein claimed. Claim 7 as herein resubmitted claims, inter alia, **in sequence,** laminating a film on an active surface of a semiconductor chip, producing holes in the film to expose contact pads on the active surface of the semiconductor chip, and filling the holes with an electrically conductive material.

In contrast, the cited Akhavain et al. patent discloses at col. 4, lines 17-49, that initially a patterned photoresist layer 12e is formed by covering parts 12c and 12d of th interconnect member 12 with an unpatterned layer of photoresist, exposing the unpatterned photoresist layer to ultraviolet light through a mask which blocks the light over just the input/output pads 12d, and removing the unexposed photoresist, thereby producing the holes, thereafter, the openings in the photoresist layer 12e are filled with a solder paste 12f'.

More particularly, claim 7 claims that the film is laminated on an active surface of a semiconductor chip whereas the cited Akhavain et al. patent discloses that the patterned photoresist film layer 12e is formed by covering the interconnect member. Claim 7 claims that holes are produced in the film thereby exposing contact pads on the active surface of the chip whereas the Akhavain et al. patent discloses that unexposed photoresist over input/output pads 12d of interconnect member 12 is removed thereby producing holes exposing the input/output pads of the interconnect member.

For the foregoing reasons Applicants respectfully submit that the method of claim 7 differs from the method disclosed in the Akhavain et al. patent and therefore respectfully submit that the identical invention is not shown in as complete detail as contained in the claim. Therefore, in accordance with *Richardson*, Applicants respectfully submit that the Akhavain et al. patent does not

anticipate the currently claimed method and therefore submit that claim 7 is patentable thereover. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 10, dependent from claim 7, is asserted to be patentable over the cited Akhavain et al. patent for at least the same reasons as claim 7. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 19

Claim 19 has been amended to clarify that the recited method steps are performed in the particular sequence therein claimed. Claim 19 as herein resubmitted claims, inter alia, laminating a film on a substrate having discrete solder bumps thereon.

In contrast, the cited Akhavain et al. patent discloses at col. 4, lines 18-35 that initially a patterned photoresist layer 12e is formed by covering parts 12c and 12d of an interconnect member 12 with an unpatterned layer of photoresist, exposing the unpatterned photoresist layer to ultraviolet light through a mask which blocks the light over just the input/output pads 12d, and removing the unexposed photoresist. Thereafter, the openings in the photoresist layer 12e are filled with a solder paste 12f' by pushing the solder paste 12f' into the openings with a squeegee. Subsequently, the structure is subjected to a high temperature for a predetermined time interval in order to vaporize and remove a portion of the solder paste 12f' leaving fillets 12f.

Applicants respectfully submit that in the presently claimed

invention the solder bumps must necessarily be present on the substrate before the film is laminated thereon so as to give meaning to the preamble term "*...in sequence*" and to give meaning to the claimed term "*... having discrete solder bumps thereon*". In contrast, in the method disclosed in the Akhavain et al. patent the film must necessarily be applied to the substrate before solder past 12f' can be placed into the holes formed therein and similarly before the solder paste can be subjected to a high temperature to form fillets 12f.

Applicants respectfully submit that the method steps as disclosed in the Akhavain et al. patent are not arranged as required by claim 19 and therefore in accordance with *In re Bond* the Akhavain et al. patent does not anticipate the currently claimed method. Applicants therefore submit that claim 19 is patentable over the Akhavain et al. patent. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 21

Claim 21 has been amended to clarify that the recited method steps are performed in the particular sequence therein claimed. Claim 21 as herein resubmitted claims, inter alia, laminating a film on an active surface of a semiconductor chip having discrete solder bumps thereon.

In contrast, the cited Akhavain et al. patent discloses at

col. 4, lines 18-64 that initially a patterned photoresist layer 12e is formed by covering parts 12c and 12d of an interconnect member 12 with an unpatterned layer of photoresist, exposing the unpatterned photoresist layer to ultraviolet light through a mask which blocks the light over just the input/output pads 12d, and removing the unexposed photoresist. Thereafter, the openings in the photoresist layer 12e are filled with a solder paste 12f' by pushing the solder paste 12f' into the openings with a squeegee. Subsequently, the structure is subjected to a high temperature for a predetermined time interval in order to vaporize and remove a portion of the solder paste 12f' leaving fillets 12f. Following the above steps, an integrated circuit chip 11 having solder bumps 11c attached to its input/output pads 11b is placed on top of the structure.

To fabricate the solder bumps 11c on the chip 11, a stencil is placed on the chips such that openings in the stencil expose just the input/output pads 11b; solder paste is pushed through the stencil openings onto the input/output pads 11b; the stencil is lifted off of the chip 11; and the solder is heated until it forms a ball due to surface tension. Thereafter, the input/output pads 11b on the chip 11 are aligned with the input/output pads 12d of the interconnect member 12 by sliding the chip 11 in random directions until the solder bumps 11c drop into the holes of photoresist layer 12e.

Applicants respectfully submit that in the presently claimed

invention the solder bumps must necessarily be present on the semiconductor chip befor the film is laminated thereon so as to give meaning to the preamble term "... *in sequence*" and to give meaning to the claimed term "... *having discrete solder bumps thereon*".

Applicants respectfully submit that Akhavain et al. nowhere discloses laminating a film on an active surface of a semiconductor chip having discrete solder bumps thereon. To the contrary, Akhavain et al. discloses that its stencil is laminated to the integrated circuit in order to facilitate thereafter fabricating the solder bumps. Applicants therefore submit that claim 21 is patentable over the Akhavain et al. patent. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 22

Claim 22 has been amended to clarify that the recited method steps are performed in the particular sequence therein claimed. More particularly, claims 22 recites performing, **in sequence**, the steps of laminating, coating, placing, curing, and reflowing.

In contrast, the cited Gutierrez et al. patent discloses at col. 5, lines 28-35 that: initially, a chip is affixed to a carrier as shown in FIG. 2, with the interconnection pads 7 reflowed to interconnect with solder balls 5. The liquid non-stick coating 9 is then dispensed underneath the chip 1 into cavity 2 by spraying, or

the like. This thin liquid non-stick coating 9 forms a film which inhibits the adhesion of the subsequently applied and cured rigid polymer encapsulant 11. That is, Gutierrez et al. discloses performing, in sequence, the steps of: affixing, reflowing, dispensing, placing, and curing.

In the Gutierrez et al. patent the step of affixing a chip to a substrate is specifically disclosed to be a first step whereas in claim 22 as amended the step of placing the chip on the substrate occurs after a film has been laminated to the chip and an encapsulent portion has been applied thereto. In the Gutierrez et al. patent solder is reflowed to electrically connect the chip to the substrate before the film and encapsulent are applied. In contrast, in claim 22 as amended the solder is the film and encapsulent are applied to the chip before the solder is reflowed.

Applicants respectfully submit that as amended the method steps as disclosed in the Gutierrez et al. patent are not arranged as required by claim 22 and therefore in accordance with *In re Bond* the Gutierrez et al. patent does not anticipate the currently claimed method. Applicants therefore submit that claim 22 is patentable over the Gutierrez et al. patent. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

Rejection under 35 U.S.C. § 103

Claim 11 was rejected as obvious over the Akhavain et al. '546

patent in view of the Nelson '308 patent; and claims 8, 16, and 20 were rejected as obvious over the Akhavain et al. '546 patent in view of the Pasch '624 patent.

RESPONSE

Claims 16 and 20 have been canceled thereby rendering their rejections moot. Applicants respectfully traverse the remaining rejections.

With respect to the rejections of claims 8 and 11, dependent from claim 7, Applicants incorporate herein by reference the arguments presented above in response to the rejection of claim 7, and respectfully submit that since claim 7 is patentable over the cited references claims 8 and 11 are likewise patentable thereover.

Newly Submitted Claims

Newly submitted independent claim 23 together with claims 24-30 dependent therefrom, and independent claim 31 together with claims 32-38 dependent therefrom, are asserted to be patentable over the prior art of record because none of the prior art references disclose a first portion encapsulant comprises a chemical composition selected so as to not adversely affect properties of a second portion encapsulent, the properties including: a fluxing agent promoting wetting of the solderable contact pads by the solder; chemically immobilizing the fluxing agent and flux reaction byproducts after cure; having a low

viscosity during a soldering operation that does not impede flow of molten solder; resisting corrosion and resisting degradation at soldering temperatures; and not evolving any gases that can cause voids or bubbles.

MISCELLANEOUS

The references cited by the Examiner have been reviewed and it is submitted that the claims as herein resubmitted are patentable thereover.

CONCLUSION

In light of the foregoing, Applicants submit that the application is in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

Respectfully submitted,

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